

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

EKNER *et al.*

Appl. No.: 09/788,670

Filed: February 21, 2001

For: **Binary Polynomial Multiplier**

Confirmation No.: 6040

Art Unit: 2193

Examiner: Do, Chat C.

Atty. Docket: 1778.2110000 (0113.00US)

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicants have listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent

application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3):

Document FP1 (JP 10-11289 A) describes an instruction number expansion method in parallel processor, and parallel processors, as indicated by its English language abstract, which is enclosed as the cover page of the document.

Document FP2 (JP 11-003226) describes a visual instruction set for CPU having integrated graphics function, as shown by the English abstract enclosed as document NPL2.

Document FP3 (JP 11-174955) describes an open key ciphering device, open key ciphering and deciphering device, and deciphering program recording medium, as shown by the English abstract enclosed as document NPL3.

Document FP4 (JP 2000-293507) describes a device and method for generating expression data in operation of finite field, as shown by the English abstract enclosed as document NPL4.

Document FP5 (JP 2000-321979) describes a polynomial arithmetic device, for calculating order of elliptic curve, device for generating elliptic curve, and cryptographic system for elliptic curve, as shown by the English abstract enclosed as document NPL5.

Document FP6 (JP 1995-182142 A) describes a polynomial multiplication circuit, for ensuring effective multiplication even when the coefficients of a polynomial are inputted en bloc by constructing plural arithmetic elements in a one-dimensional array, as shown by the English abstract enclosed as NPL16.

Copies of documents FP1-FP6; NPL1-NPL16 are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the attached IDS Forms are submitted.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in black ink, appearing to read "David C. Isaacson", with a long horizontal flourish extending to the right.

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Date: April 20, 2009

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